FIG.1

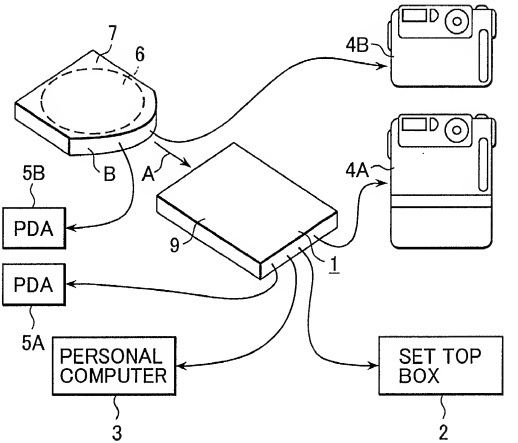


FIG.2A

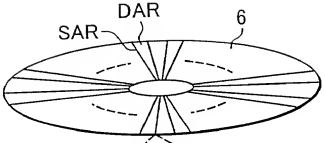

DAR
SAR
6

FIG.2B

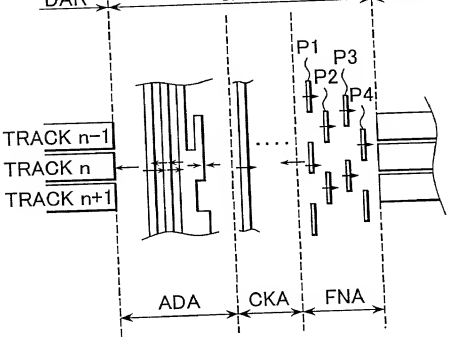

DAR
SAR
DAR
P1
P2
P3
P4
TRACK n−1
TRACK n
TRACK n+1
ADA
CKA
FNA

FIG.3

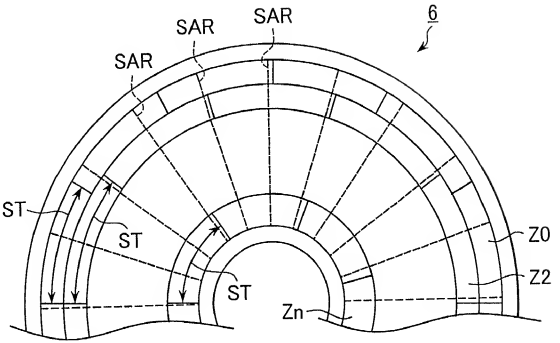


FIG.4

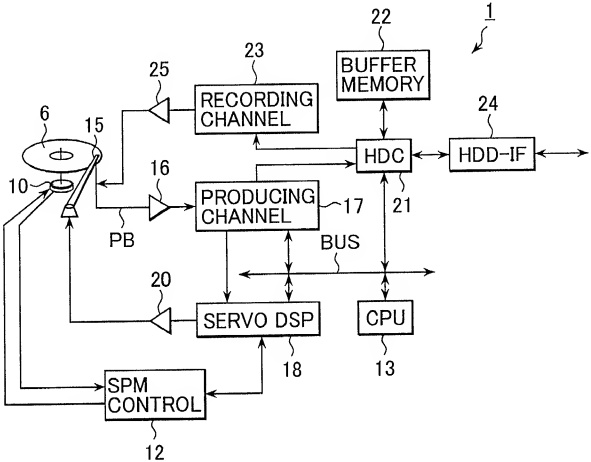

1
22
BUFFER MEMORY
23
25
RECORDING CHANNEL
24
HDD-IF
6
15
HDC
16
10
PRODUCING CHANNEL
17
21
PB
BUS
20
SERVO DSP
CPU
18
13
SPM CONTROL
12

FIG.5

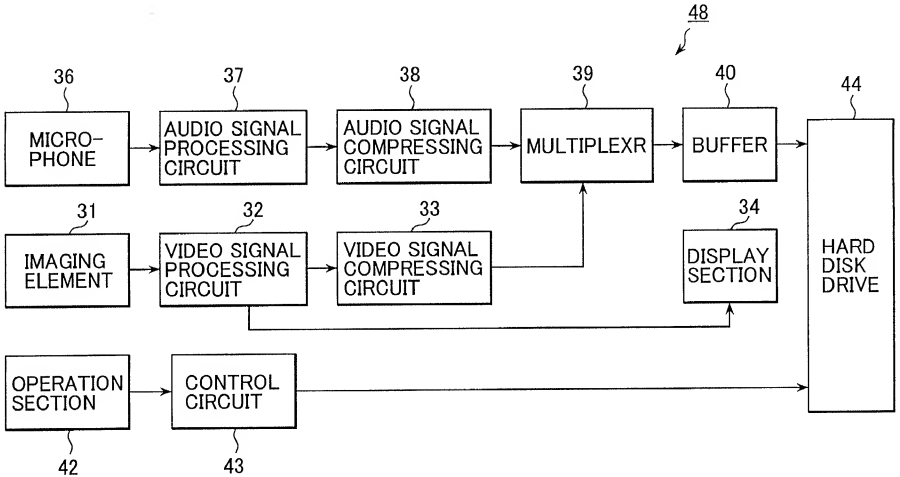
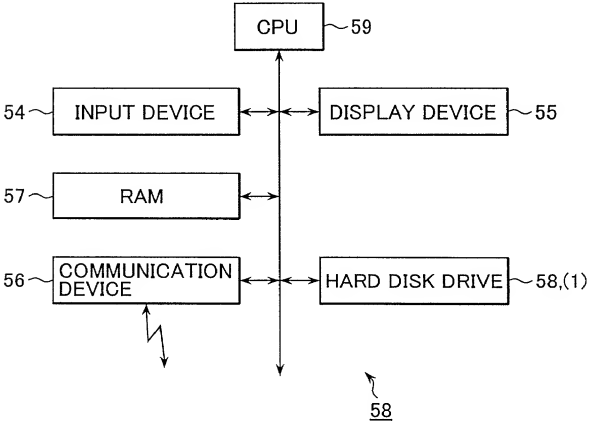

48
36
MICRO-PHONE
37
AUDIO SIGNAL PROCESSING CIRCUIT
38
AUDIO SIGNAL COMPRESSING CIRCUIT
39
MULTIPLEXR
40
BUFFER
44
HARD DISK DRIVE
31
IMAGING ELEMENT
32
VIDEO SIGNAL PROCESSING CIRCUIT
33
VIDEO SIGNAL COMPRESSING CIRCUIT
34
DISPLAY SECTION
OPERATION SECTION
42
CONTROL CIRCUIT
43

FIG.6


CPU
59
54
INPUT DEVICE
DISPLAY DEVICE
55
57
RAM
56
COMMUNICATION DEVICE
HARD DISK DRIVE
58,(1)
58